# Cache paramaters

A Haswell machine has a 44-bit physical address space, 32-kB L1 data cache, 8-way set associative, 64-bytes per line.

32kB cache (2^15), 8-way (2^3), line size 64(2^6), 44-bit physical address space (2^44)

## How many bits are used to calculate the offset?

Offset= log2(linesize)=6 bits

## How many bits are used to calculate the line?

Lines=log2((cachesize/ways)/linesize)=6 bits

## How many bits are used for the tag?

Tag= addresssize-(offset bits +line bits)=44-12=32 bits

# Cache problem

This question assumes a 512-byte cache, 16-bytes per line, 2-way associative, 32-bit address size. (24 bits of tag, 4 bits for line, 4 bits for offset).

For each of the following memory accesses state whether it is a cache hit or miss, and if it’s a miss state whether the old contents of the cache have to be written back to memory or not.

## ldrb r0, 0x0000080f

line 0, offset f, tag 000008, way 0 is the last recent use, comparing the tag is a conflict miss. It should not be written back to memory.

## ldrb r0, 0xffffffff

line f, offset f, tag ffffff. Either way 0 or way 1 is not having any value stored in cache. So it is a cold miss. The old contents of the cache should not be written back to memory.

## strb r0, 0x00000810

line 1, offset 0, tag 000008. The tag value does not match the last recent use way 1 tag value 00000a, it is a conflict miss. It is a store instruction, so it will be written back to memory.

# Bzip2 cache behavior on the x86 Haswell Machine

For this section, log into the Haswell machine just like in previous homeworks. Run the bzip2 benchmark, recall you will use a command line something like this:

perf stat -e instructions:u,L1-icache-load-misses:u /opt/ece571/401.bzip2/bzip2 -k -f ./input.source

## Measure and report the L1 instruction cache miss rate.

Use instructions:u and L1-icache-load-misses:u for the events.

Performance counter stats for '/opt/ece571/401.bzip2/bzip2 -k -f ./input.source':

19,161,578,173 instructions:u

122,026 L1-icache-load-misses

3.618405904 seconds time elapsed

Miss rate: 122026/19161578173=6.4\*10^-6

## Measure and report the L1 data cache load miss rate.

Use L1-dcache-loads:u and L1-dcache-load-misses:u

Performance counter stats for '/opt/ece571/401.bzip2/bzip2 -k -f ./input.source':

6,244,598,662 L1-dcache-loads

311,555,584 L1-dcache-load-misses # 4.99% of all L1-dcache hits

3.417852789 seconds time elapsed

Miss rate: 311555584/6244598662=4.99% miss rate.

## Measure and report the L3 cache miss rate

Use cache-references:u and cache-misses:u

Performance counter stats for '/opt/ece571/401.bzip2/bzip2 -k -f ./input.source':

140,266,397 cache-references:u

793,076 cache-misses:u # 0.565 % of all cache refs

3.416443955 seconds time elapsed

Miss rate: 793076/140266397=0.565%

# equake\_l cache behavior on the x86 Haswell Machine

Recall that running equake looks something like this:

perf stat -e instructions:u,L1-icache-load-misses:u /opt/ece571/equake\_l.specomp/equake\_l < /opt/ece571/equake\_l.specomp/inp.in

## Measure and report the L1 instruction cache miss rate.

## Use instructions:u and L1-icache-load-misses:u for the events.

Performance counter stats for '/opt/ece571/equake\_l.specomp/equake\_l':

1,424,807,601,994 instructions:u

14,801,557 L1-icache-load-misses

134.332496479 seconds time elapsed

Miss rate: 14801557/1424807601994=1.04\*10^-5

## Measure and report the L1 data cache load miss rate.

## Use L1-dcache-loads:u and L1-dcache-load-misses:u

Performance counter stats for '/opt/ece571/equake\_l.specomp/equake\_l':

526,540,941,299 L1-dcache-loads

30,673,158,032 L1-dcache-load-misses # 5.83% of all L1-dcache hits

134.495297462 seconds time elapsed

Miss rate: 30673158032/526540941299=5.83%

## Measure and report the L1 data cache store miss rate.

## Use L1-dcache-stores:u and L1-dcache-store-misses:u

Performance counter stats for '/opt/ece571/equake\_l.specomp/equake\_l':

140,445,521,440 L1-dcache-stores

<not supported> L1-dcache-store-misses

134.479730125 seconds time elapsed

## Measure and report the L3 cache miss rate

## Use cache-references:u and cache-misses:u

Performance counter stats for '/opt/ece571/equake\_l.specomp/equake\_l':

13,711,669,950 cache-references:u

8,134,974,766 cache-misses:u # 59.329 % of all cache refs

137.064356682 seconds time elapsed

Miss rate= 8134974766/13711669950=59.329%

# Bzip2 cache behavior on the Jetson

## For icache rate try measuring r14:u (which is L1\_ICACHE) and r01:u (which is L1I\_CACHE\_REFILL).

Performance counter stats for '/opt/ece571/401.bzip2/bzip2 -k -f ./input.source':

20,141,621,035 instructions:u

10,494,701,853 r14:u

170,105 r01:u

10.478125410 seconds time elapsed

Icache rate= 10494701853/20141621035=52.1%

## Measure and report the L1 data cache load miss rate.

## Use r40:u (which is L1D\_CACHE\_LD) and r42:u (which is L1D\_CACHE\_REFILL\_LD).

Performance counter stats for '/opt/ece571/401.bzip2/bzip2 -k -f ./input.source':

20,141,621,035 instructions:u

6,022,423,496 r40:u

252,781,245 r42:u

10.488030122 seconds time elapsed

L1 data cache load miss rate= 252781245/6022423496=4.20%

## Measure and report the L1 data cache store miss rate.

## Use r41:u (which is L1D\_CACHE\_ST) and r43:u (which is L1D\_CACHE\_REFILL\_ST).

Performance counter stats for '/opt/ece571/401.bzip2/bzip2 -k -f ./input.source':

20,141,621,035 instructions:u

2,223,252,798 r41:u

56,163,695 r43:u

10.547978150 seconds time elapsed

Miss rate= 56163695/2223252798=2.53%

# Measure and report the L2 data cache load miss rate.

# Use r50:u (which is L2D\_CACHE\_LD) and r52:u (which is L2D\_CACHE\_REFILL\_LD).

Performance counter stats for '/opt/ece571/401.bzip2/bzip2 -k -f ./input.source':

20,141,621,035 instructions:u

326,998,312 r50:u

28,978,705 r52:u

10.492802263 seconds time elapsed

Miss rate= 28978705/326998312=8.86%

# Measure and report the L2 data cache store miss rate.

# Use r51:u (which is L2D\_CACHE\_ST) and r53:u (which is L2D\_CACHE\_REFILL\_ST).

Performance counter stats for '/opt/ece571/401.bzip2/bzip2 -k -f ./input.source':

20,141,621,035 instructions:u

308,972,622 r51:u

21,623,373 r53:u

10.444435925 seconds time elapsed

Miss rate=21623373/308972622=7.00%

# Short Answer Questions

## How do the various cache miss rates for bzip2 compare between the Haswell and the Jetson?

|  |  |  |
| --- | --- | --- |
| Bzip2 | X86 Haswell | ARM64 Jetson |
| L1 instruction cache miss rate | 6.4\*10^-6 |  |
| L1 data cache load miss rate | 4.99% | 4.20% |
| L3 cache miss rate | 0.565% |  |
| Icache rate |  | 52.1% |
| L1 data cache store miss rate |  | 2.53% |

The cache miss rate is similar for the L1 data cache load miss rate.

## How do the various cache miss rates on the Haswell machine compare between the bzip2 and equake benchmarks?

|  |  |  |
| --- | --- | --- |
| Haswell machine | Bzip2 | equake |
| L1 instruction cache miss rate | 6.4\*10^-6 | 1.04\*10^-5 |
| L1 data cache load miss rate | 4.99% | 5.83% |
| L3 cache miss rate | 0.565% | 59.329% |
| L1 data cache store miss rate |  | Not support |

The cache miss rate is similar for the L1 instruction and data cache miss rate. But not for the L3 cache miss rate.